

Fig. 1

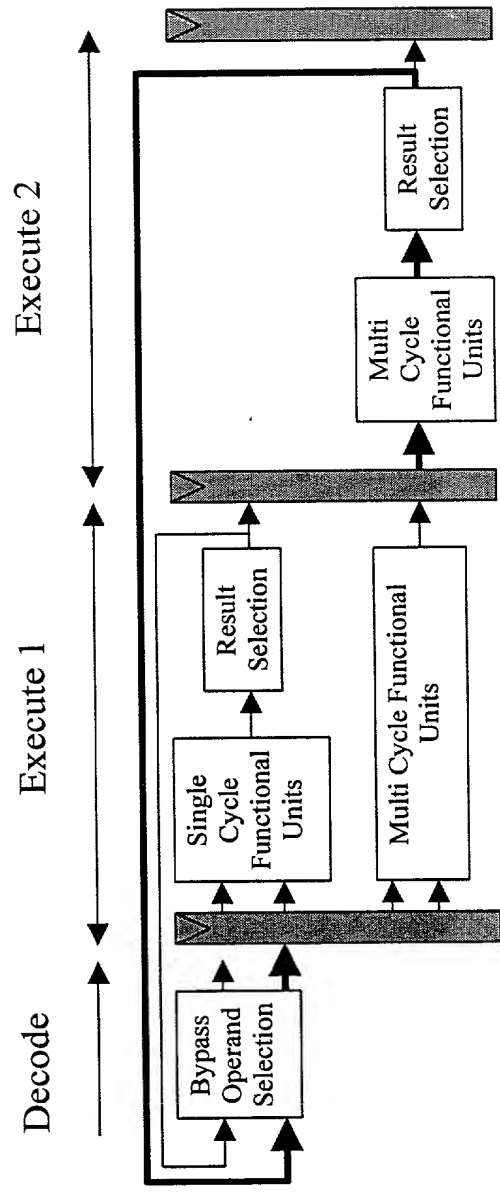


Fig. 2

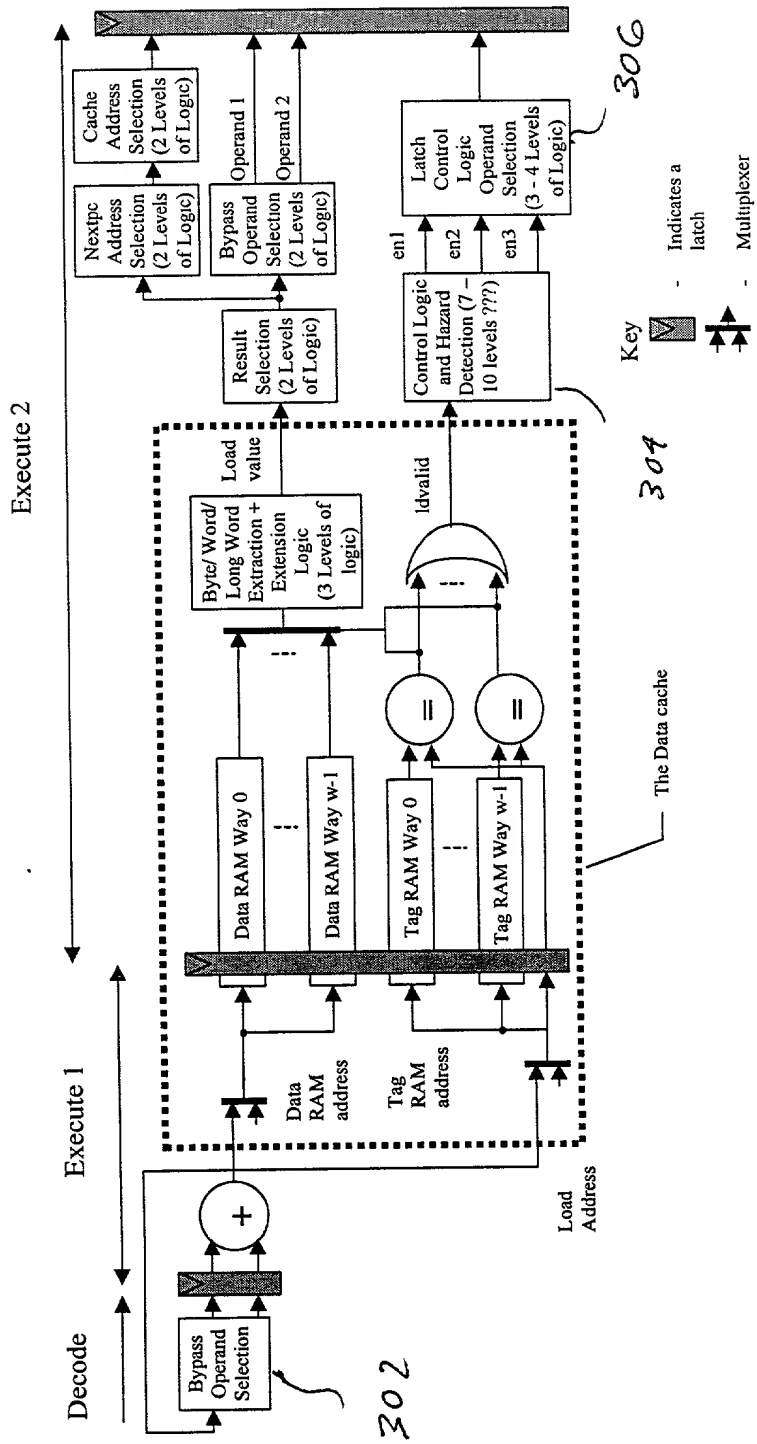


Fig. 3

**Fig. 3a.**

Pipeline Stage						
Reference Step	0	F	D	E1	E2	WB
350	Ld					
352	Mov	Ld				
354	Add	Mov	Ld			
356		Add	Mov	Ld		
358			Add	Mov	Ld	
360			Add		Mov/Ld	
362			Add		Ld	Mov
364				Add		Ld
366					Add	
368						Add

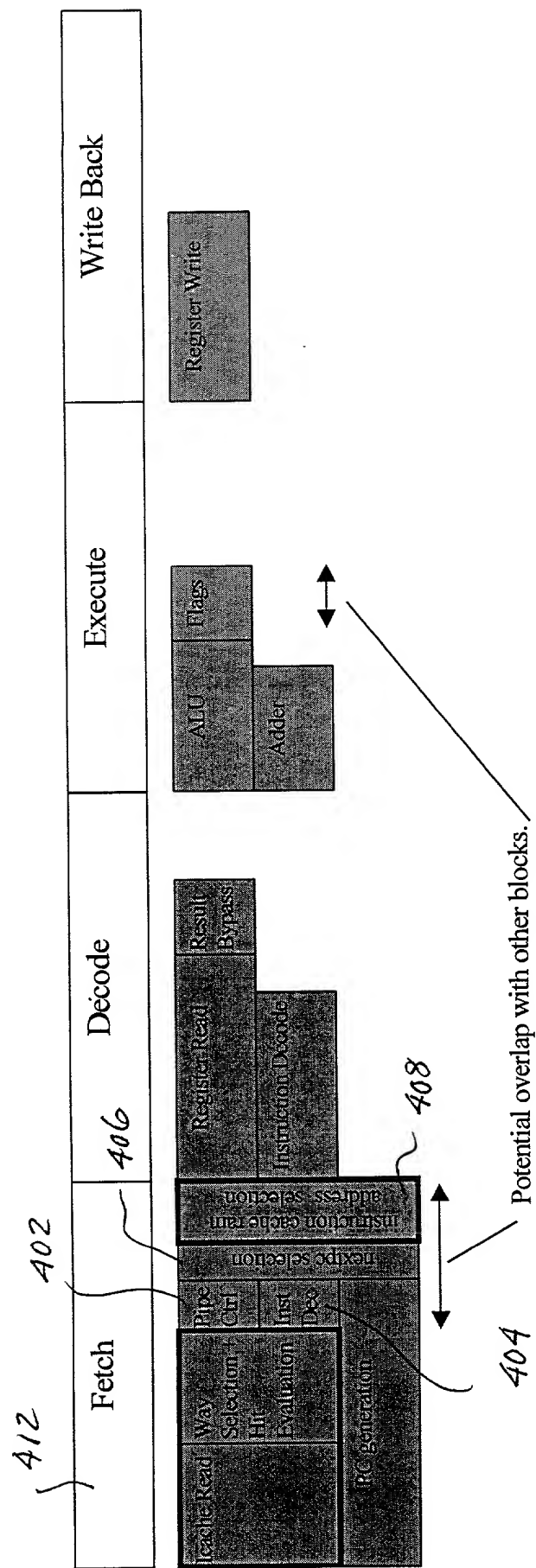


Fig. 4



FIG. 5

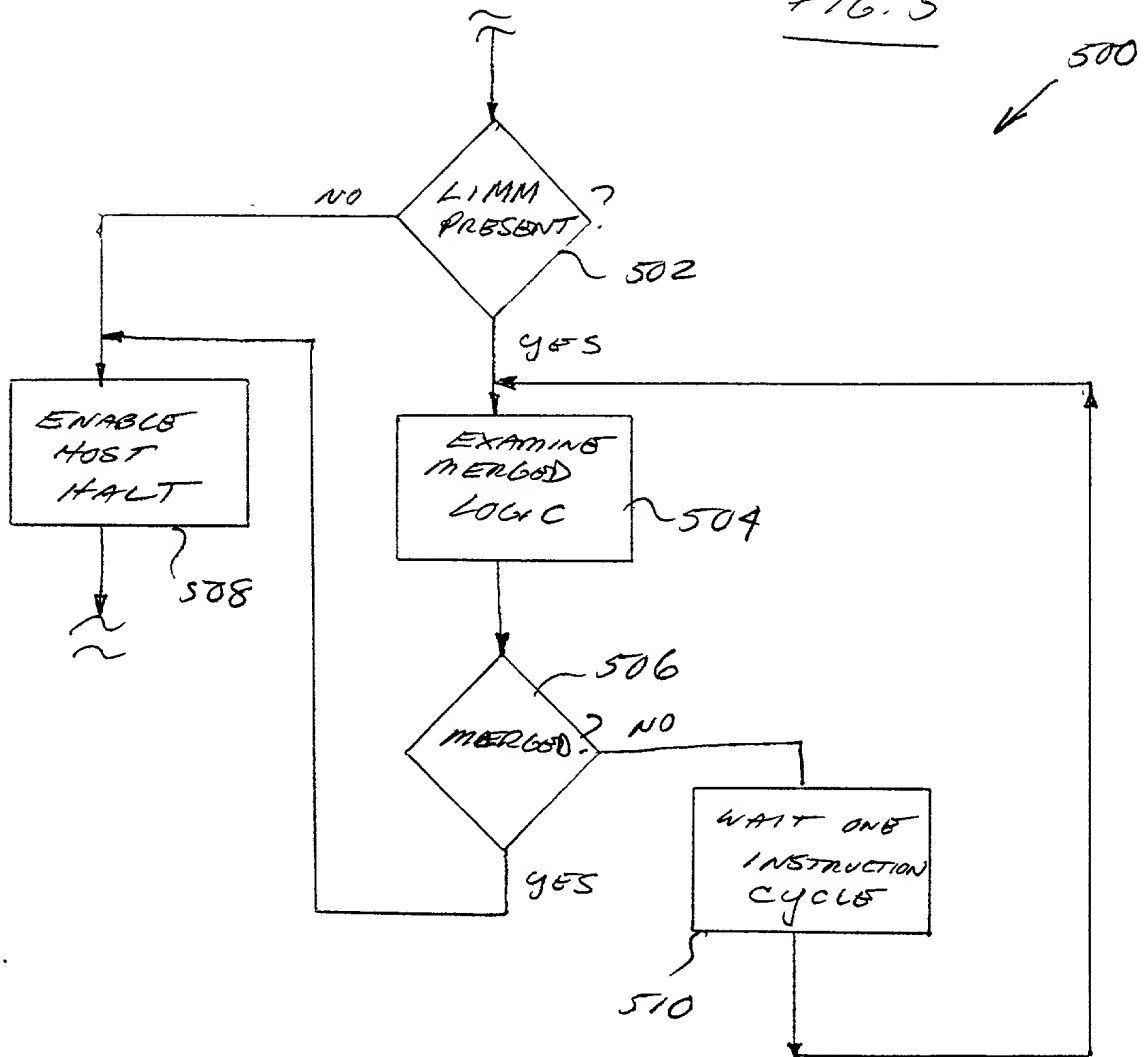


FIG. 6 is a block diagram of a processor pipeline. The pipeline is divided into four stages: Fetch, Decode, Execute, and Write Back. The Fetch stage includes a PC Read block (602) and a Branch Prediction block (604). The Decode stage includes a Register Read block (610) and an Instruction Decode block (610). The Execute stage includes an ALU block (606) and a Result Bypass block (606). The Write Back stage includes a Register Write block (606).

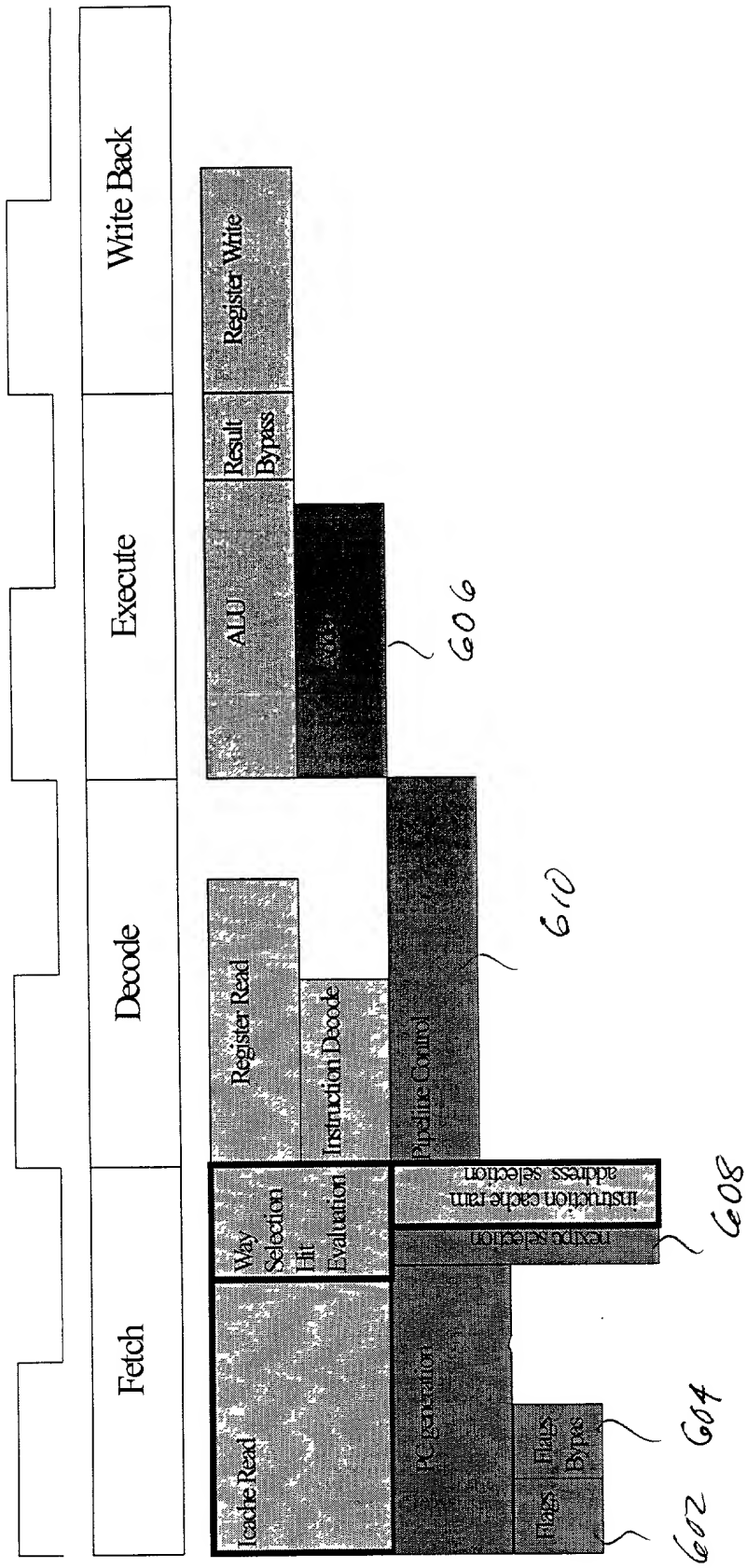


Fig. 6



1. The present invention relates to a data path architecture for a processor, and more particularly to a data path architecture for a processor that includes a pipeline.

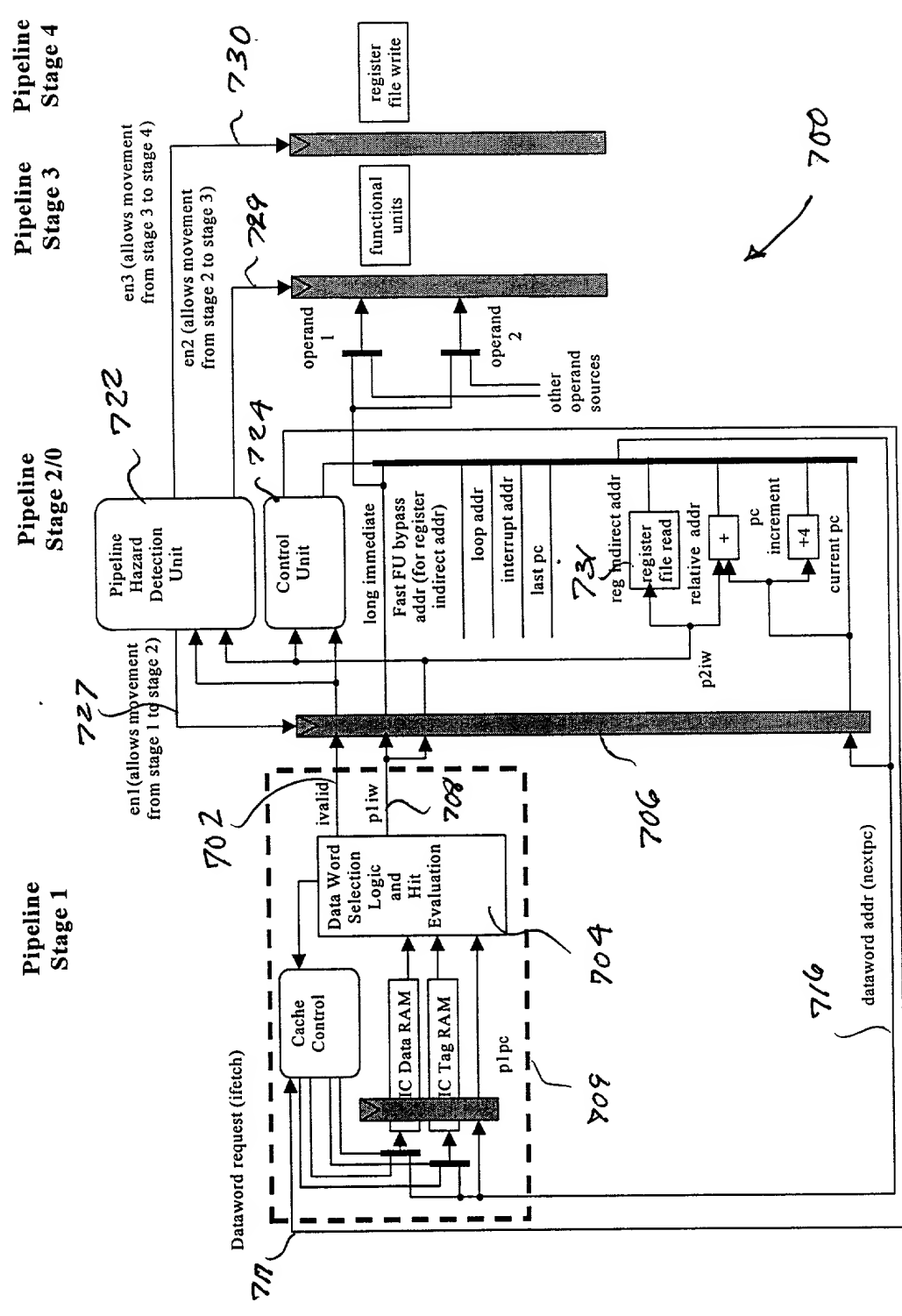


Fig. 7

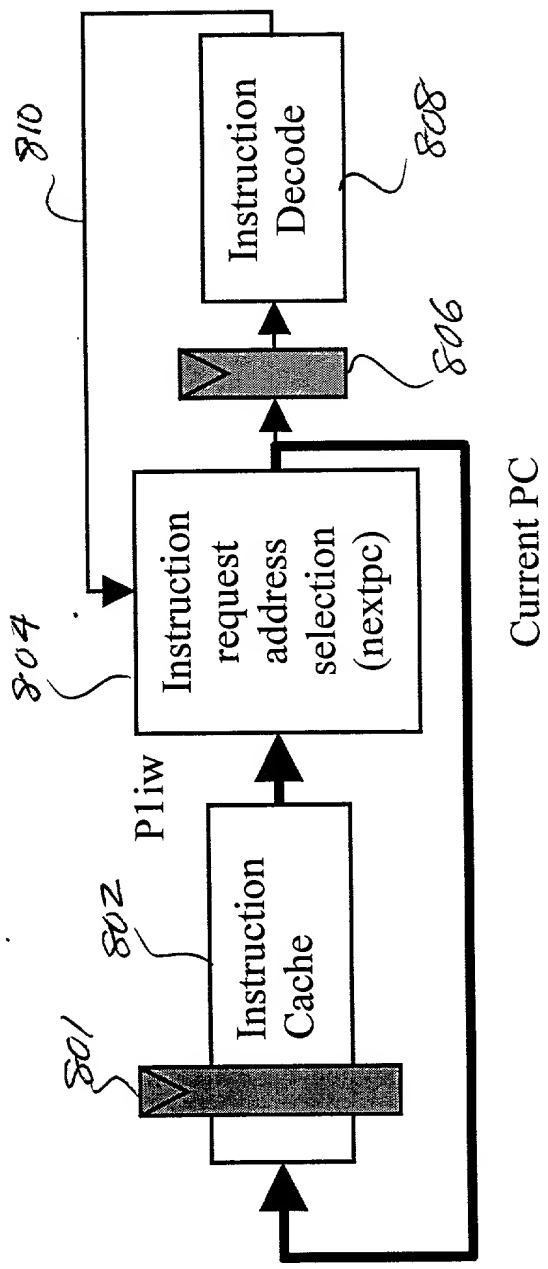


Fig. 8

800

**Fig. 8a**

Reference Step	Instruction Fetch Address (Inst Addr: next_pc)	Pipeline Stage			
		Fetch (Inst Addr: current_pc)	Decode (Inst Addr: last_pc)	Execute	Write- back
820	J.d <sub>A</sub>				
822	Brk <sub>B</sub>	J.d <sub>A</sub>			
824	Target <sub>C</sub>	Brk <sub>B</sub>	J.d <sub>A</sub>		
826		Target <sub>C</sub>	Brk <sub>B</sub>	J.d <sub>A</sub>	
828			Brk		J.d <sub>A</sub>
			Restart		
830			Brk		
			Restart		
832	Add <sub>B</sub>		Brk		
			Restart		
834	Target <sub>C</sub>	Add <sub>B</sub>			
836	Target <sub>2C</sub>	Target <sub>C</sub>	Add <sub>B</sub>		
838	Target <sub>3C</sub>	Target <sub>2C</sub>	Target <sub>C</sub>	Add <sub>B</sub>	

**Fig. 8b**

Reference Step	Instruction Fetch Address (Inst Addr: next_pc)	Pipeline Stage			
		Fetch (Inst Addr: currentpc)	Decode (Inst Addr: last_pc)	Execute	Write-back
840	Add <sub>A</sub>				
842	Brk <sub>B</sub>	Add <sub>A</sub>			
844	Mov <sub>C</sub>	Brk <sub>B</sub>	Add <sub>A</sub>		
846		Mov <sub>C</sub>	Brk <sub>B</sub>	Add <sub>A</sub>	
848			Brk Restart		Add <sub>A</sub>
850			Brk Restart		
852	Add <sub>B</sub>		Brk Restart		
854	Mov <sub>C</sub>	Add <sub>B</sub>			
856	Mov2 <sub>C</sub>	Mov <sub>C</sub>	Add <sub>B</sub>		
858	Mov3 <sub>C</sub>	Mov2 <sub>C</sub>	Mov <sub>C</sub>	Add <sub>B</sub>	

**Fig. 8c**

Reference	Instruction Fetch Address (Inst Addr: next_pc)	Pipeline Stage			
		F (Inst Addr: currentpc)	D (Inst Addr: last_pc)	E	W
860	J.d <sub>A</sub>				
862	Brk <sub>B</sub>	J.d <sub>A</sub>			
864	Target <sub>C</sub>	Brk <sub>B</sub>	J.d <sub>A</sub>		
866		Target <sub>C</sub>	Brk <sub>B</sub>	J.d <sub>A</sub>	
868			Brk		
870			Restart		
			Brk	J.d <sub>A</sub>	
872	Add <sub>B</sub>		Restart		
			Brk	J.d <sub>A</sub>	
874	Target <sub>C</sub>	Add <sub>B</sub>		J.d <sub>A</sub>	
876	Target <sub>2C</sub>	Target <sub>C</sub>	Add <sub>B</sub>	J.d <sub>A</sub>	
878	Target <sub>3C</sub>	Target <sub>2C</sub>	Target <sub>C</sub>	Add <sub>B</sub>	J.d <sub>A</sub>

FIG. 9 is a block diagram of a processor 900 showing two execution units, Execute 1 and Execute 2, and their associated functional units and result selection units.

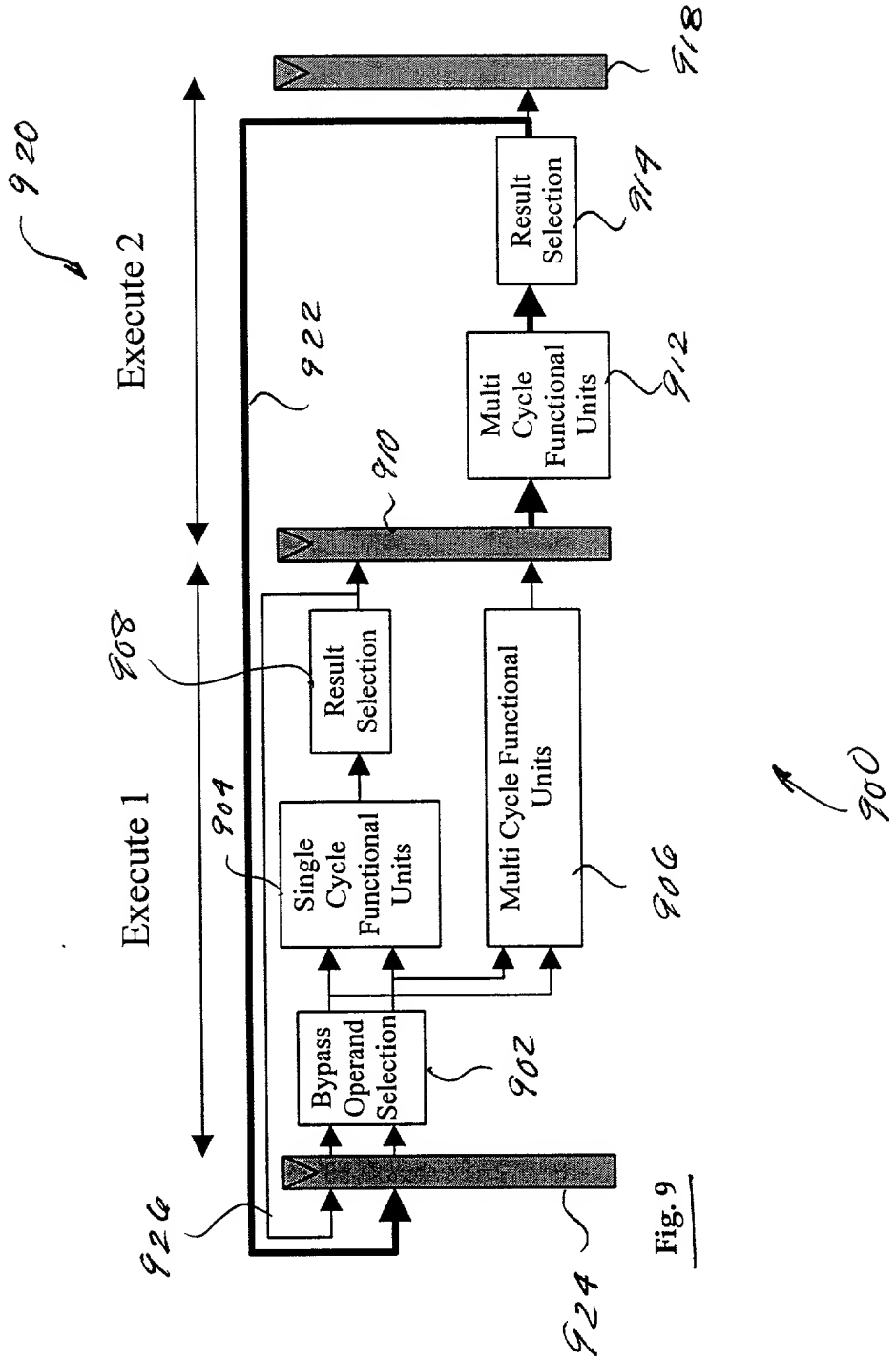


Fig. 9

F76.10

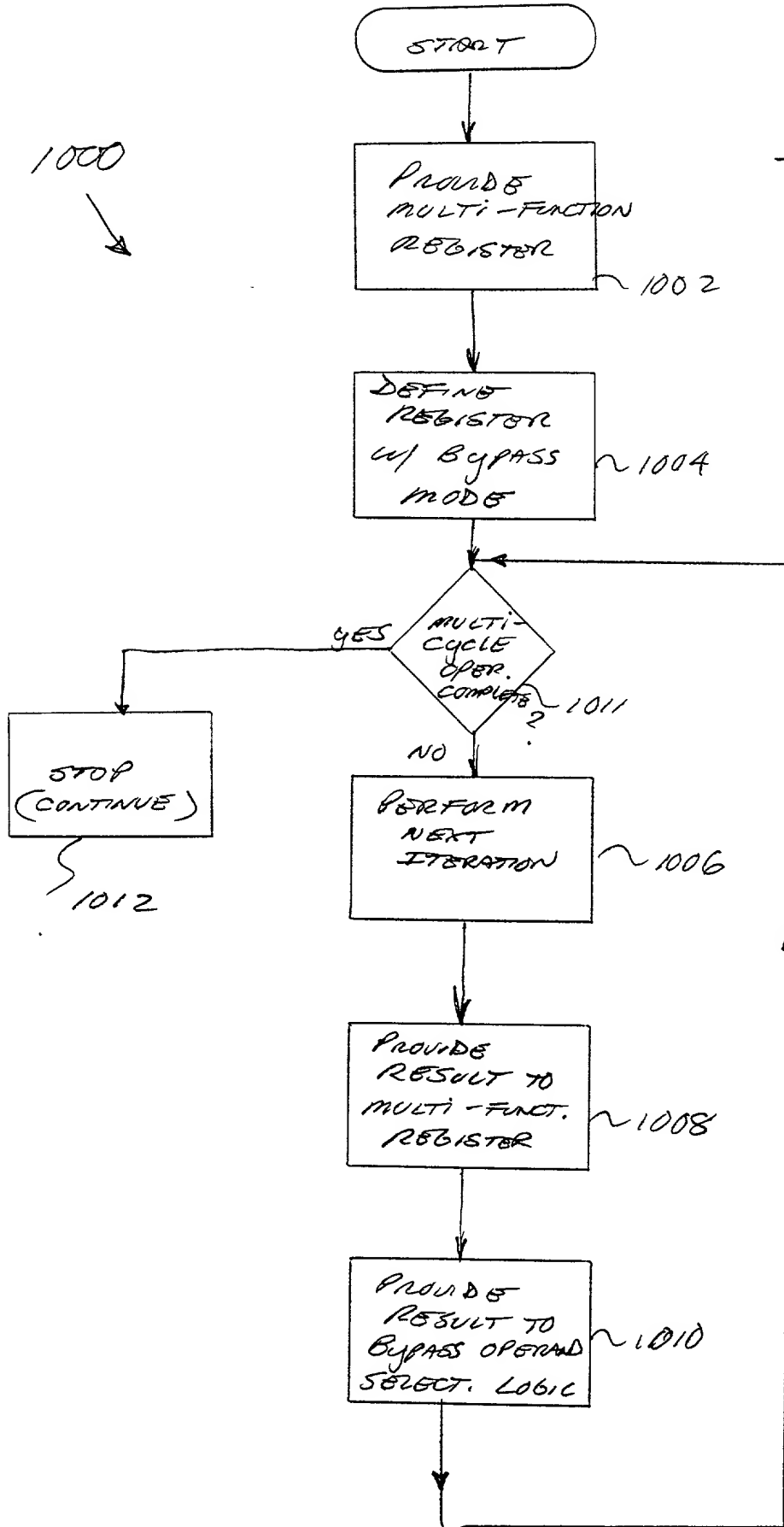


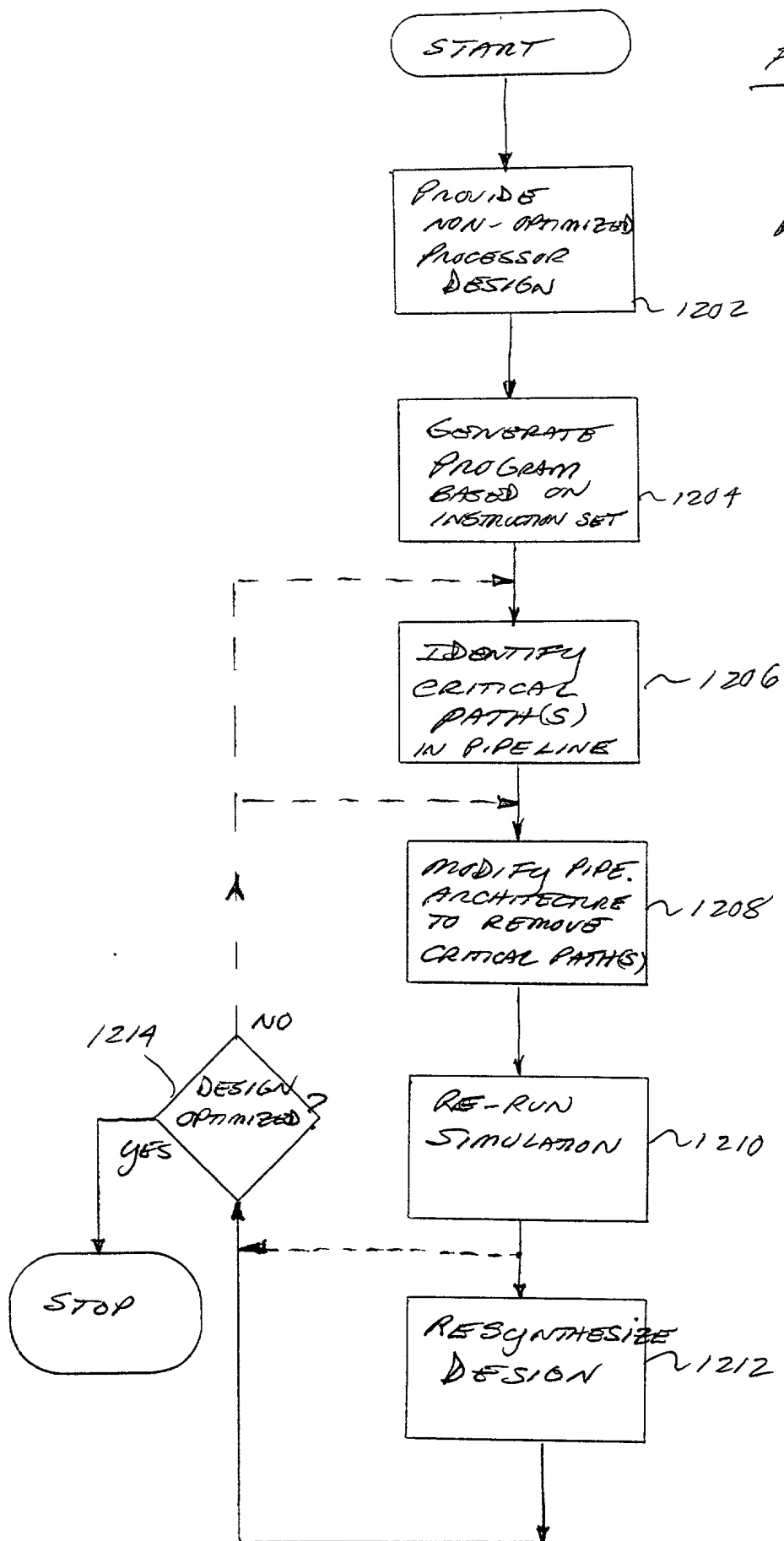




Fig. 11a

Pipeline Stage						
Reference	0	F	D	E1	E2	WB
1174	Ld					
1176	Mov	Ld				
1178	Add	Mov	Ld			
1180		Add	Mov	Ld		
1182			Add	Mov	Ld	
1184				Add	Mov/Ld	
1186				Add	Ld	Mov
1188				Add		Ld
1190				Add	Add	
1192						Add

FIG. 12



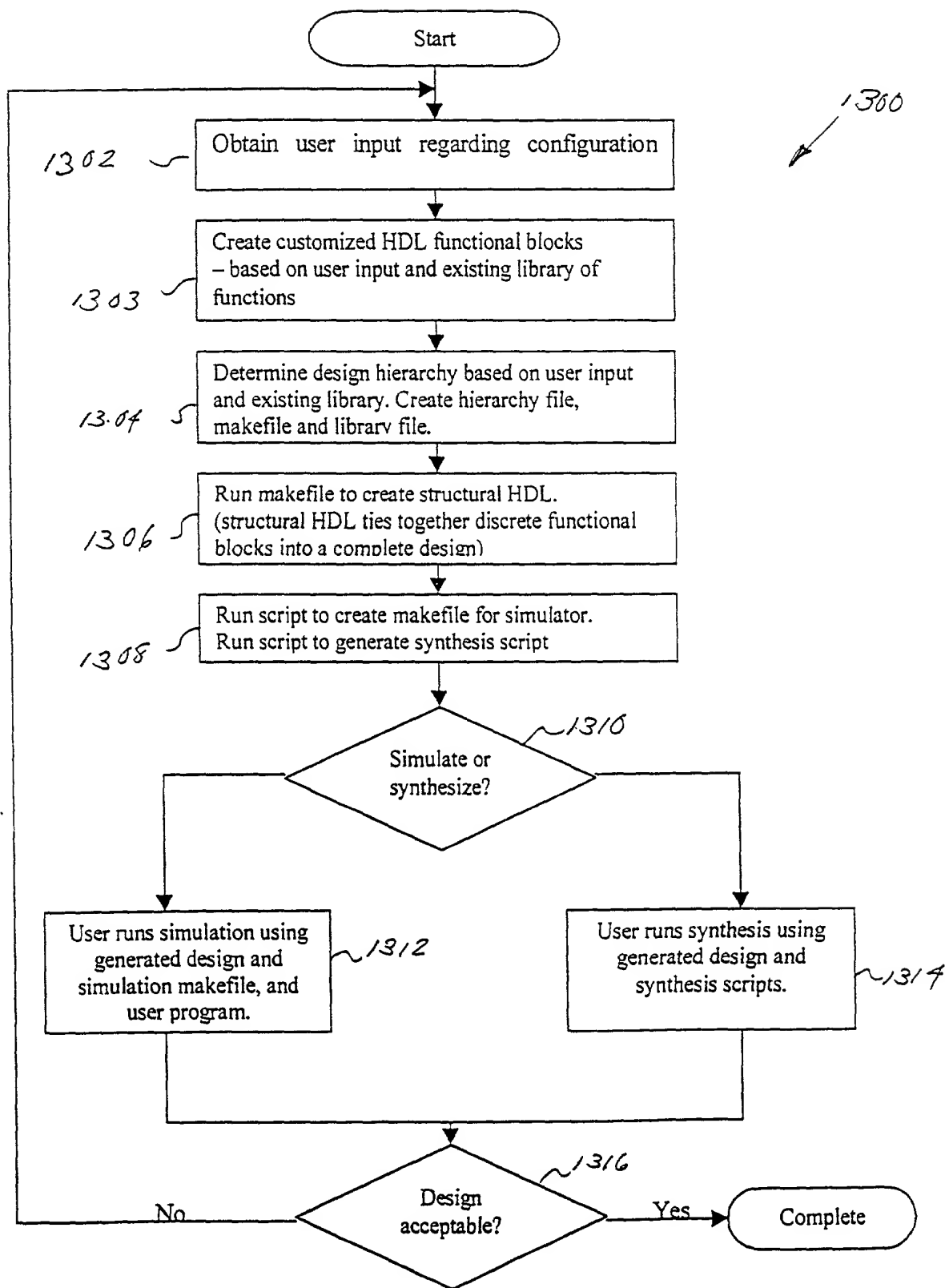


FIG. 13

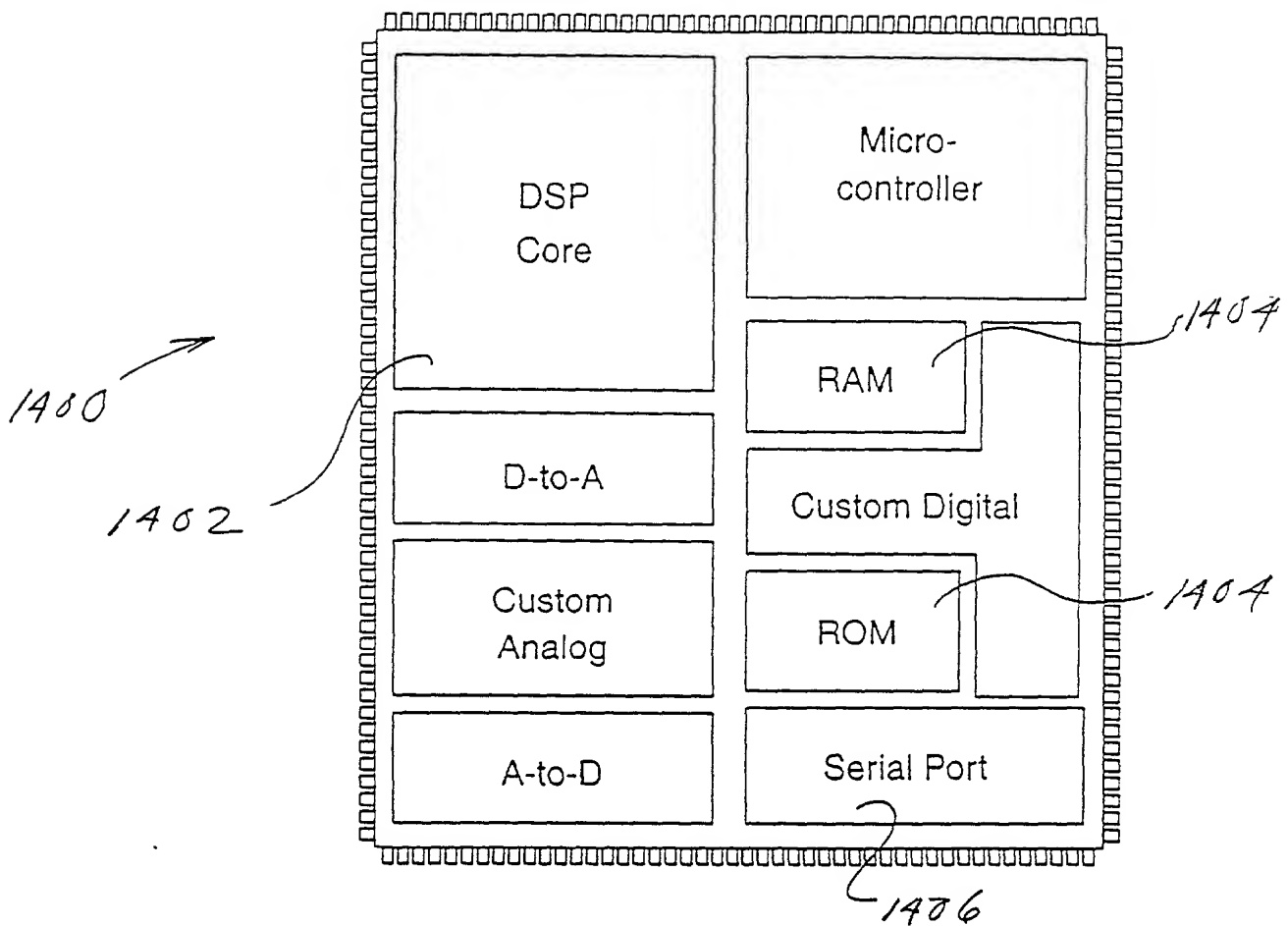


FIG. 1A

[illegible]